REMARKS

Reconsideration of the application is requested.

Claims 1-9 and 11-14 remain in the application. Claims 1-9 and 11-14 are subject to examination.

Under the heading "Claim Rejections – 35 USC § 103" on page 2 of the above-identified Office Action, claims 1-3, 7-9, 11, and 12 have been rejected as being obvious over U.S. Patent No. 5,541,541 to Salamina et al. in view of Published U.S. Patent Application No. 2001/0026490 to Nakagawa under 35 U.S.C. § 103. Applicant respectfully traverses.

Claim 1 defines a receiver circuit including a detector circuit having first and second signal detectors;

> said first and second signal detectors each having a control input for setting the detection threshold to at least a first value and a second value lower than the first value; and
>
> after an amplitude of one of the first and second input signals exceeds the first value of the detection threshold, the detection threshold compared to another one of the first and second input signals being decreased to the second value of the detection threshold.

Claim 12 defines a receiver circuit including a detector circuit connected to said first input and said second input and providing detector output signals dependent on a comparison of the first and second input signals with a

detection threshold settable to at least a first value and a second value lower than the first value, said detector output signals include a first detector output signal and a second detector output signal, after one of the first and second input signals exceeds the first value of the detection threshold, the detection threshold compared to another one of the first and second input signals being decreased to the second value of the detection threshold.

The Examiner has recognized that Salamina et al. do not teach the features of claims 1 and 12 copied above. The Examiner, however, has alleged that Nakagawa teach such features and Nakagawa suggests an obvious modification to the circuit taught in Salamina et al.

Applicant first asserts that such a modification would not have been obvious because it would have rendered the circuit in Salamina et al. inoperable for the intended purpose.

Let us first discuss the teaching in Salamina et al. Figure 4 of Salamina et al. shows a circuit for controlling transistors 12, 14 that are connected in series. These transistors 12, 14 are controlled using first and second control circuits 20, 22. These control circuits 20, 22 receive control signals HSDin, LSDin, which control the transistors 12, 14. Each of the control circuits 20, 22 further-receives a signal that is dependent on the output signal of the other control circuit.

Notably, the control circuits 20, 22 are adapted to switch on the corresponding

transistor 12, 14 only, if the corresponding control signal HSDin, LSDin has an on-signal level, and if the output signal of the other control circuit indicates that the other transistor is switched off. In other words - one of the control circuits 20, 22 allows an on-signal level of corresponding control signal HSDin, LSDin to pass to the control terminal of the corresponding transistor 12, 14 only in those cases in which the signal that is dependent on the output signal of the other control circuit indicates that the other transistor is switched off. The control circuits 20, 22 may be considered as detectors that have two threshold levels: a first threshold level that is low enough to let an on-signal level of the corresponding control signal to pass to the transistor; and a second threshold level that prevents an on-signal level of the corresponding control signal from passing to the transistor. The threshold level of one control circuit is dependent on the output signal of the other control circuit.

If one considers the control circuits 20 and 22 of Salamina et al. to be detectors that compare input signals HSDin, LSDin to detection thresholds, the function of this circuit is quite contrary to the function of the circuit in claims 1 and 12. In the circuit of Salamina et al., the threshold of a first one of the control circuits 20, 22 is set high after an on-signal level of the control signal received by a second one of the control circuits has been detected. Setting the threshold of the first control circuit to high prevents an on-signal level of the control signal received by this first control circuit to be detected; i.e. to be passed to the transistor.

If, for some reason, one of ordinary skill in the art were to reduce this threshold level (as specified in claims 1 and 12) - both transistors 12, 14 would be allowed to switch on simultaneously. This would be hazardous and totally contrary to the teaching and to the entire purpose of Salamina et al. of only allowing one transistor to be switched on at any given time (See column 2, lines 34-37 and lines 13-19). Therefore such a modification would not have been obvious and the claimed invention would not have been obtained.

Let us now consider the teaching of Nakagawa in detail. Nakagawa teaches a sense amplifier for sensing the data in a memory cell. Nakagawa teaches that memory cells may be defective only at a high or low temperature and that therefore these defective memory cells will not be identified during the usual testing at room temperatures (paragraph 0008). Nakagawa teaches a sense amplifier for determining, at room temperature, which memory cells would become defective at a high or low temperature (paragraph 0033). For this purpose three types of reference cells are provided to generate different reference voltages RAT, RAH, RAL (paragraphs 0021-0022). The differential circuit operates at room temperature and compares the output voltage SA from the memory cell amplifier with the reference voltages RAH and RAL to determine whether the selected memory cell will function properly at the high or low temperature (paragraph 0029).

Applicant believes it has been clearly shown that the circuit taught by Salamina et al. could not have been modified in the manner asserted by the Examiner.

Additionally, however, even if the circuit taught by Salamina et al. could have been modified in the manner asserted by the Examiner, Nakagawa does not provide any such motivation for doing so. The Examiner has stated that the motivation for the modification to Salamina et al. would have been to determine whether the output voltage would be high or low as taught by Nakagawa.

Nakagawa in no way suggests any type of modification to the output circuit of Salamina et al. Nakagawa teaches providing multiple reference voltages for the purpose of determining whether a memory cell will be functional at a high or low operating temperature. The purpose is not to determine "whether the output voltage would be high or low" as stated by the Examiner. Providing multiple reference voltages in order to test the functionality of a memory cell has absolutely nothing to do with the totem pole output circuit taught by Salamina et al. One of ordinary skill in the art considering the teachings would find nothing in the teaching of Nakagawa suggesting a modification to the output circuit of Salamina et al.

Still further, paragraph 0011 of Nakagawa does not teach or suggest the following claimed limitation: after one of the first and second input signals exceeds the first value of the detection threshold, the detection threshold compared to another one of the first and second input signals being decreased to the second value of the detection threshold. That paragraph simply refers to the embodiment shown in Fig. 3 that has multiple differential circuits in which each one of the differential circuits is provided with one of the different

reference voltages (see paragraph 0040).

Under the heading "Claim Rejections – 35 USC § 103" on page 5 of the above-identified Office Action, claim 4 has been rejected as being obvious over U.S. Patent No. 5,541,541 to Salamina et al. in view of Published U.S. Patent Application No. 2001/0026490 to Nakagawa and further in view of U.S. Patent No. 4,953,070 to Lenz under 35 U.S.C. § 103. Applicant respectfully traverses.

Even if Lenz did teach the subject matter alleged by the Examiner, and even if there were a suggestion to modify the circuit in Salamina et al. because of the teaching in Lenz, the claimed invention could not have been obtained for the reasons given above with regard to claim 1 and the teachings in Salamina et al. and Nakagawa.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 12. Claims 1 and 12 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 12.

Finally, applicant appreciatively acknowledges the Examiner's statement that claims 5, 6, 13, and 14 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In

light of the above, applicants respectfully believe that rewriting of claims 5, 6, 13, and 14 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-9 and 11-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

/Laurence A. Greenberg/
Laurence A. Greenberg
(Reg. No. 29,308)

MPW:cgm

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Lerner Greenberg Stemer LLP
P.O. Box 2480
Hollywood, Florida 33022-2480
Tel.: (954) 925-1100
Fax: (954) 925-1101